

Official Amendment

Serial No. 10/056,610

Docket : MIO 0051 V2/40509.183

IN THE CLAIMS

This listing of claims will replace all prior versions, and lists, of claims in the application:

- 1-29. (canceled)
30. (previously amended) A method of encapsulating an integrated circuit comprising:
providing a semiconductor chip;
providing a laminate defining first and second major faces, said laminate including an
upper electrically conductive layer at said first major face, an underlying resin
laminate substrate supporting said upper electrically conductive layer, and a lower
electrically conductive layer at said second major face;
forming at least one void in said laminate so as to extend from one of said major faces
through said upper electrically conductive layer into said underlying resin
laminate substrate, but not as far as said lower electrically conductive layer and
said second major face; and
encapsulating said semiconductor chip and said laminate with an encapsulant such that
said encapsulant extends into said void to contact said underlying substrate.
31. (canceled)
32. (currently amended) A method of forming a laminate to lock an encapsulant comprising:
~~providing forming~~ a lower continuous conductive layer;
~~providing forming~~ at least one continuous resin laminate layer over said lower continuous
conductive layer-;
~~providing forming~~ a second resin laminate layer over said continuous resin laminate layer,
so as to define an underlying cavity in said second resin laminate layer;

Official Amendment

Serial No. 10/056,610

Docket : MIO 0051 V2/40509.183

~~providing forming~~ a third resin laminate layer over said second resin laminate layer, so as to define a void portion in said third resin laminate layer over said underlying cavity;

~~providing forming~~ a fourth resin laminate layer over said third resin laminate layer, so as to define a void portion in said fourth resin laminate layer over said void portion of said third resin laminate layer;

~~providing forming~~ an upper conductive layer over said fourth resin laminate layer, so as to define a void portion in said upper conductive layer over said void portion of said fourth resin laminate layer; and

~~providing forming~~ a solder resist layer over said upper conductive layer, so as to define a void portion in said solder resist layer over said void portion of said upper conductive layer, wherein each said void portion taken together defines a void which does not extend as far as said lower continuous conductive layer.

33. (previously amended) The method of claim 32, wherein said underlying cavity, said void portion of said third resin laminate layer, said void portion of said fourth resin laminate layer, said void portion of said upper conductive layer and said void portion of said solder resist layer are formed to collectively form a void.

34. (previously presented) The method of claim 33 further comprising:
placing a die over at least a portion of said solder resist layer; and
forming an encapsulant over said solder resist layer, over said die and in said void.

35-39. (canceled)

Official Amendment

Serial No. 10/056,610

Docket : MIO 0051 V2/40509.183

40. (currently amended) A method of encapsulating an integrated circuit comprising:
providing a die;
providing a substrate having at least one continuous lower conductive laminate layer and
at least one resin layer over said continuous lower conductive laminate layer;
~~providing forming~~ at least one upper conductive laminate layer over said at least one resin
layer;
forming a void in said at least one resin layer and said at least one upper conductive
laminate layer such that a portion of said void located in said at least one resin
layer is below a remaining portion of said at least one upper conductive laminate
layer, wherein said void does not extend as far as through ~~through~~ said continuous lower
conductive laminate layer;
placing said die over said at least one upper conductive laminate layer; and
encapsulating said die by forming encapsulant over said at least one upper conductive
laminate layer, over said die and in said void.
41. (previously amended) The method of claim 40, wherein said at least one upper
conductive laminate layer is formed by forming a conductive layer over said at least one resin
layer and forming a solder resist layer over said conductive layer.
42. (previously amended) The method of claim 40, wherein said void is formed by forming
an underlying cavity in said at least one upper conductive laminate layer.
43. (previously presented) The method of claim 40, wherein said encapsulant is formed in
substantially all of said void.
44. (previously presented) The method of claim 40, wherein said at least one resin layer is
formed from bismaleimide triazine laminate.

Official Amendment

Serial No. 10/056,610

Docket : MIO 0051 V2/40509.183

45. (previously presented) The method of claim 40, wherein said at least one resin layer is formed from FR-4 epoxy-glass laminate.
- 46-49. (canceled)
50. (previously presented) The method of claim 33, wherein said void has a varying profile.
51. (previously presented) The method of claim 50, wherein said void having a varying profile is formed by a process selected from the group consisting of drilling, stamping, chemical etching, and combinations thereof.
52. (previously presented) The method of claim 50, wherein said void having a varying profile is formed having a T-shaped profile.
53. (previously amended) The method of claim 33, wherein said void extends into said resin laminate, but not entirely through said continuous resin laminate layer.